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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/886,741 | 06/21/2001 | Vincent Chan | ATI.0100680 | 6028 |

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| EXAMINER | |
|---|---|
| CHU, CHRIS C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/886,741 | CHAN ET AL. | |
| | Examiner | Art Unit | |
| | Chris C. Chu | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) *10,14,19,22,26,42,50,52 and 62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 - 9, 11 - 13, 17, 18, 20, 23 - 25, 41, 44 - 48, 53, 54, 56 - 61 and 63 - 67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/05 & 1/3/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 2 - 14, 17 - 20, 22 - 26, 41 - 42, 44 - 48, 50, 52-54 and 56 - 67.

## DETAILED ACTION

### *Request for Continued Examination*

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 3, 2006 has been entered. An action on the RCE follows.

### *Response to Amendment*

2. Applicant's amendment filed on January 3, 2006 has been received and entered in the case.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 65 – 67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(A) In claim 65, line 1, "the semiconductor die" lacks antecedent basis.

(B) In claim 66, line 1, "the semiconductor die" lacks antecedent basis.

(C) In claim 67, line 1, "the semiconductor die" lacks antecedent basis.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 4 – 6, 8, 9, 12, 13, 41, 44 – 46, 48, 54, 56, 58, 60, 63 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tutsch et al. (U. S. Pat. No. 6,630,727) in view of Sudo et al. (U. S. Pat. No. 5,475,264).

Regarding claim 56, Tutsch et al. discloses in e.g., Fig. 2 a device comprising:

- a package module (a device in Fig. 2) including a substrate (2; column 7, line 30) having a standard package footprint;
- an unpackaged semiconductor die (the right-side chip 1; see Fig. 2 and column 7, line 34) attached to the package module (see Fig. 2), the unpackaged semiconductor die encapsulated (12; column 8, line 8) onto the package module in a structure having a planar top surface (see Fig. 2); and
- a separately packaged semiconductor die (the left-side chip 1 which is packaged by the element 12; see Fig. 2 and column 7, line 34) having a top surface and attached to the package module;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate (see Fig. 2).

However, Tutsch et al. does not disclose a direct attachment of the unpackaged semiconductor die on the package module. Sudo et al. teaches in e.g., Fig. 2 and column 1, lines 14 – 31 a direct attachment (the attachment without adhesive, glue or attaching material) of an unpackaged semiconductor die (23; column 4, line 30) on a package module (22; column 4, line 31). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the adhesive layer (15) under the unpackaged semiconductor chip of Tutsch et al. as taught by Sudo et al. to improve an integration density and speed of a module (column 1, lines 14 – 31).

Regarding claim 2, Tutsch et al. discloses in Fig. 2 the packaged semiconductor being packaged in a ball grid array package (see Fig. 2 and column 8, lines 2 – 3).

Regarding claims 4 and 54, Tutsch et al. discloses in e.g., Fig. 2 the packaged semiconductor die being a memory (column 4, lines 60 – 65).

Regarding claim 5, Tutsch et al. discloses in Fig. 2 and Fig. 6 a plurality of packaged semiconductors (the left-side chips 1 which are packaged by the element 12) being attached to the package module (see e.g., Fig. 2).

Regarding claim 6, Tutsch et al. discloses in e.g., Fig. 2 the unpackaged semiconductor die (the right-side chip 1) being wire bonded (10; column 7, line 42) to the package module (see Fig. 2).

Regarding claim 8, the phrase "wherein attached includes surface-mount technology reflow" is product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-

by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also ln re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and ln re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 9, Tutsch et al. discloses in e.g., Fig. 2 and Fig. 6 the encapsulated structure (the right-side chip 1) having a footprint greater than the footprint of the unpackaged semiconductor die (one of the left-side chips 1).

Regarding claims 12, 48 and 60, since the element (5) of Tutsch et al. transfers a heat, the element 5 reads as a heat sink (column 3, lines 12 – 15, column 4, lines 11 – 12 and column 7, lines 62 – 64). Thus, Tutsch et al. discloses a planar heat sink adapted to engage the encapsulated structure and the top surface of the packaged semiconductor.

Regarding claim 13, Tutsch et al. discloses in e.g., Fig. 2 a top surface of the unpackaged semiconductor die and a top surface of the packaged semiconductor being of substantially equal distance from a surface of the package module (see Fig. 2).

Regarding claim 41, Tutsch et al. discloses in e.g., Fig. 2 the encapsulated semiconductor die forming a substantially rectangular structure on the package (see Fig. 2 and Fig. 6).

Regarding claim 58, Tutsch et al. discloses in e.g., Fig. 2 a multi-die module, comprising:

- a substrate (2) having a first surface and a second surface;
- an unpackaged semiconductor die (the right-side chip 1) mounted to the first surface of the substrate, the semiconductor die encapsulated (12 and 5) in a structure having a planar top surface; and
- a packaged semiconductor die (the left-side chip 1 which is packaged by element 12) having a top surface and mounted on the first surface of the substrate;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate (see Fig. 2).

However, Tutsch et al. does not disclose a direct attachment of the unpackaged semiconductor die on the package module. Sudo et al. teaches in e.g., Fig. 2 and column 1, lines 14 – 31 a direct attachment (the attachment without adhesive, glue or attaching material) of an unpackaged semiconductor die (23; column 4, line 30) on a package module (22; column 4, line 31). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the adhesive layer (15) under the unpackaged semiconductor chip of Tutsch et al. as taught by Sudo et al. to improve an integration density and speed of a module (column 1, lines 14 – 31).

Regarding claim 44, Tutsch et al. discloses in e.g., Fig. 2 and Fig. 6 a second packaged semiconductor die (the other left-side chip 1 which is packaged by element 12; see Fig. 6) mounted on the first surface of the substrate.

Regarding claim 45, Tutsch et al. discloses in e.g., Fig. 2 and Fig. 6 a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

Regarding claim 46, Tutsch et al. discloses in e.g., Fig. 2 and Fig. 6 the unpackaged semiconductor die being mounted to the first surface of the substrate by wire bonding (10).

Regarding claims 63 and 65, Tutsch et al. discloses in e.g., Fig. 2 said unpackaged semiconductor die (the right-side chip 1) being at least partially encapsulated (12 and 5) on the package module (see e.g., Fig. 2).

7. Claims 47, 59, 61, 66 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tutsch et al. in view of Sudo et al. and further in view of Lu et al. (U. S. Pat. No. 6,294,731).

Regarding claims 47, 59 and 61, Tutsch et al. discloses in e.g., Fig. 2 a multi-die module, comprising:

- a substrate (2) having a first surface;
- an unpackaged semiconductor die (the right-side chip 1) mounted to the first surface of the substrate, the semiconductor die encapsulated (12) in a structure having a planar top surface; and
- a packaged semiconductor die (the left-side chip 1 which is packaged by element 12) having a top surface (claim 61) and mounted on the first surface of the substrate,
- wherein the encapsulating structure (12 and 5); and
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate (see Fig. 2).

However, Tutsch et al. does not disclose a direct attachment of the unpackaged semiconductor die on the package module and the material of the encapsulating structure. Sudo

et al. discloses in e.g., Fig. 2 and column 1, lines 14 – 31 a direct attachment (the attachment without adhesive, glue or attaching material) of an unpackaged semiconductor die (23; column 4, line 30) on a package module (22; column 4, line 31). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the adhesive layer (15) under the unpackaged semiconductor chip of Tutsch et al. as taught by Sudo et al. to improve an integration density and speed of a module (column 1, lines 14 – 31).

Furthermore, Tutsch et al. and Sudo et al. do not disclose a material of the encapsulating structure being metal cap (claim 47, 59 and 61). Lu et al. teaches in e.g., Fig. 1 a material of the encapsulating structure (140) being metal cap (column 7, line 55). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the metal cap of Lu et al. into the specific material to form the encapsulating structure on top of the chips of Tutsch et al. and Sudo et al. as taught by Lu et al. to provide EMI shield (column 9, line 64).

Regarding claims 66 and 67, Tutsch et al. discloses in e.g., Fig. 2 the semiconductor die (the right-side chip 1) being at least partially encapsulated (12 and 5) on the package module (see e.g., Fig. 2).

8. Claims 3, 7, 17, 18, 20, 24, 25, 53, 57 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tutsch et al. in view of Sudo et al. and further in view of Hannah '232.

Regarding claims 3, 53 and 57, Tutsch et al. discloses in e.g., Fig. 2 a device comprising:

- a package module (a structure in Fig. 2);
- a die (the right-side chip 1) attached to the package module, the die encapsulated (12 and 5) on the package module in a structure having a planar top surface; and

- a packaged memory die (the left-side chip 1which is packaged by element 12; column 4, lines 60 – 65) having a top surface and attached to the package module;
- wherein the planar top surface of the encapsulated structure and the top surface of the packaged die are of equal distance from the package module (see Fig. 2).

However, Tutsch et al. does not disclose a direct attachment of the unpackaged semiconductor die on the package module and the material of the encapsulating structure. Sudo et al. discloses in e.g., Fig. 2 and column 1, lines 14 – 31 a direct attachment (the attachment without adhesive, glue or attaching material) of an unpackaged semiconductor die (23; column 4, line 30) on a package module (22; column 4, line 31). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the adhesive layer (15) under the unpackaged semiconductor chip of Tutsch et al. as taught by Sudo et al. to improve an integration density and speed of a module (column 1, lines 14 – 31).

Furthermore, Tutsch et al. and Sudo et al. do not disclose the semiconductor dice being graphics-processor die. However, Hannah teaches in column 3, lines 42 - 46 and column 5, lines 16 - 21 semiconductor dice being a graphics-processor. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tutsch et al. and Sudo et al. by using the graphics-processor of Hannah to be the unpackaged semiconductor die of Tutsch et al. and Sudo et al. as taught by Hannah. The ordinary artisan would have been motivated to modify Tutsch et al. and Sudo et al. in the manner described above for at least the purpose of receiving commands and graphics data from the main CPU of the computer (column 3, lines 42 - 46).

Regarding claim 7, Tutsch et al. and Sudo et al., as modified, disclose the graphics processing die (the right-side chip 1) being wire bonded (10) to the package module (see Fig. 2).

Regarding claim 17, Tutsch et al. and Sudo et al., as modified, discloses a plurality of packaged memory (the left-side chips 1; see Fig. 6 of Tutsch et al.) being attached to the package module.

Regarding claim 18, Tutsch et al. and Sudo et al., as modified, discloses directly attached including the graphics processing die (the right-side chip 1) being wire bonded (10) to the package module (see Fig. 2 of Tutsch et al.).

Regarding claim 20, the phrase "wherein attached includes surface-mount technology reflow" is product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also ln re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and ln re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 24, since the element (5) of Tutsch et al. transfers a heat, the element 5 read as a heat sink (column 3, lines 12 – 15, column 4, lines 11 – 12 and column 7, lines 62 – 64). Thus, Tutsch et al. discloses a heat sink.

Regarding claim 25, Tutsch et al. and Sudo et al., as modified, disclose in e.g., Fig. 2 a top surface of the graphics-processor die and a top surface of the packaged memory being of substantially equal distance from a surface of the package module (see Fig. 2).

Regarding claim 64, Tutsch et al. and Sudo et al., as modified, disclose in e.g., Fig. 2 said graphics-processing die being at least partially encapsulated on the package module.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tutsch et al. and Sudo et al. as applied to claim 56 above, and further in view of Takano et al. '907.

Tutsch et al. and Sudo et al. disclose the semiconductor package set forth in the claims except for the standard package sizes being 40mm X 40mm. However, Takano et al. teaches in TABLE 1 a standard package sizes being 40mm X 40mm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tutsch et al. and Sudo et al. by using the standard package sizes as taught by Takano et al. The ordinary artisan would have been motivated to modify Tutsch et al. and Sudo et al. in the manner described above for at least the purpose of reducing a limitation in the size of a semiconductor chip (column 2, lines 6 and 7).

10. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tutsch et al., Sudo et al. and Hannah as applied to claim 57 above, and further in view of Takano et al.

Tutsch et al., Sudo et al. and Hannah disclose the semiconductor package set forth in the claims except for the standard package sizes being 40mm X 40mm. However, Takano et al. teaches in TABLE 1 a standard package sizes being 40mm X 40mm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Tutsch et al., Sudo et al. and Hannah by using the standard package sizes as taught by Takano et al. The ordinary artisan would have been motivated to further modify Tutsch et al., Sudo et al. and Hannah in the manner described above for at least the purpose of reducing a limitation in the size of a semiconductor chip (column 2, lines 6 and 7).

### *Response to Arguments*

11. Applicant's arguments with respect to claims 56 – 59 and 61 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dalal et al. discloses a packaged chip and unpackaged chip.

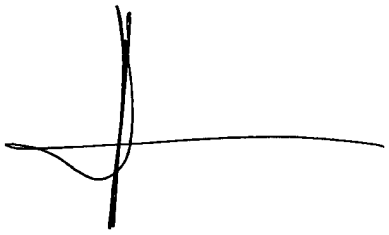
13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Thursday, January 19, 2006



KENNETH PARKER
SUPERVISORY PATENT EXAMINER